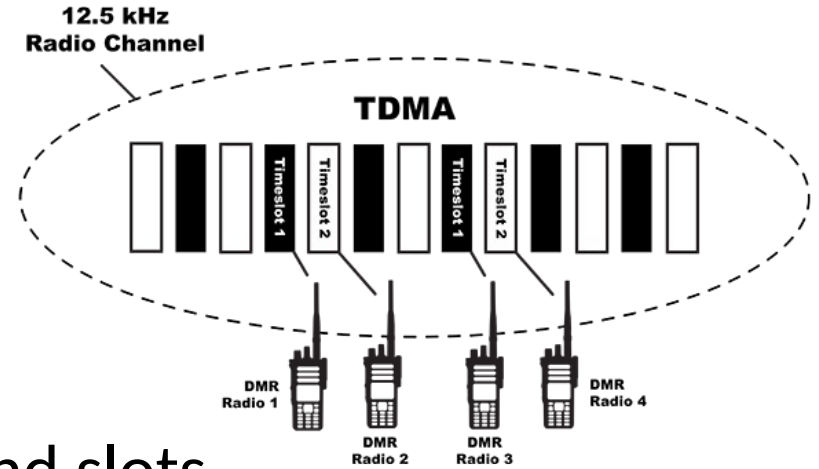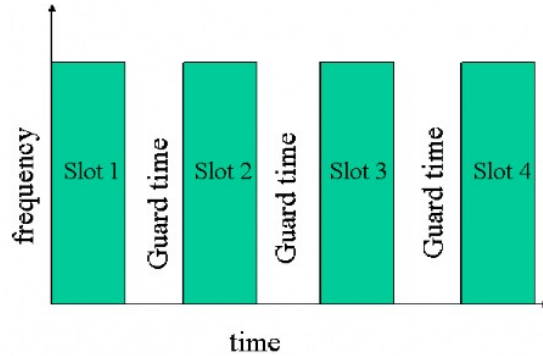# Design Considerations for Time-Slotted LoRa(WAN)

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Ireland

# Time-slotted communications





- Time is divided in repeated frames and slots

- The nodes are synchronised according to a global clock

- Guard times are added to tolerate slight desynchronisations

- Examples: GSM, IEEE802.15.4e-TSCH, WirelessHART etc.

# LoRa and LoRaWAN

- Proprietary spread spectrum modulation

- Trades data rate with sensitivity (distance)

- (almost orthogonal) Spreading Factors (SF) from 7 to 12

- Higher SF → longer range but lower data rate, longer transmission time, and higher energy consumption

- Open source protocol proposed by LoRa Alliance

- ALOHA-based MAC

- Registration, security, roaming, and localisation mechanisms for LoRa devices

- 8+1 channels, 125kHz bandwidth (EU)
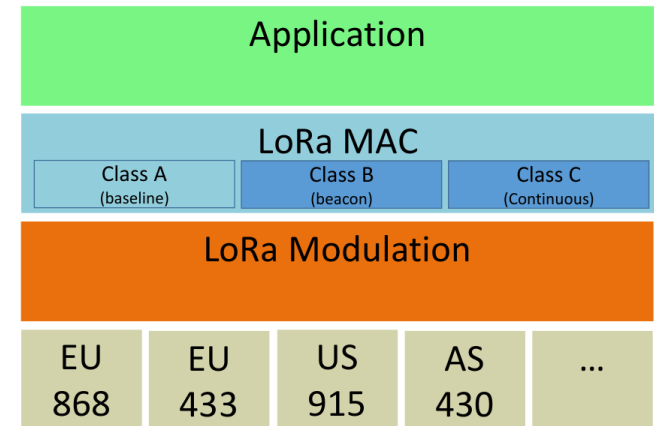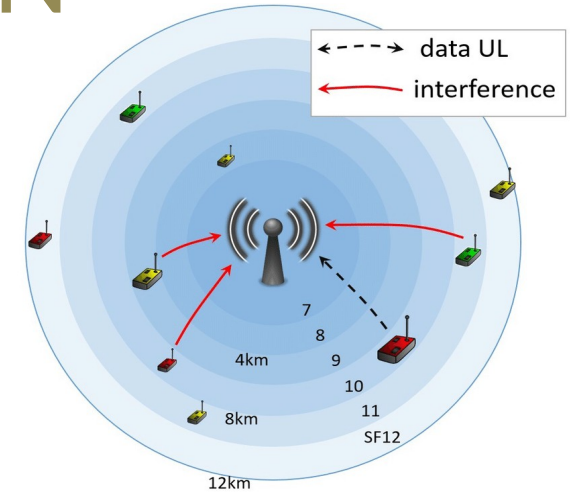
# Why Time-Slotted LoRa(WAN)?

- Performance guarantees

  ○ delay, packet delivery

- Long-range

  ○ No routing, decreased cost, increased mobility

- Industrial IoT applications

  ○ Frequent packet transmission

  ○ Reliable communications
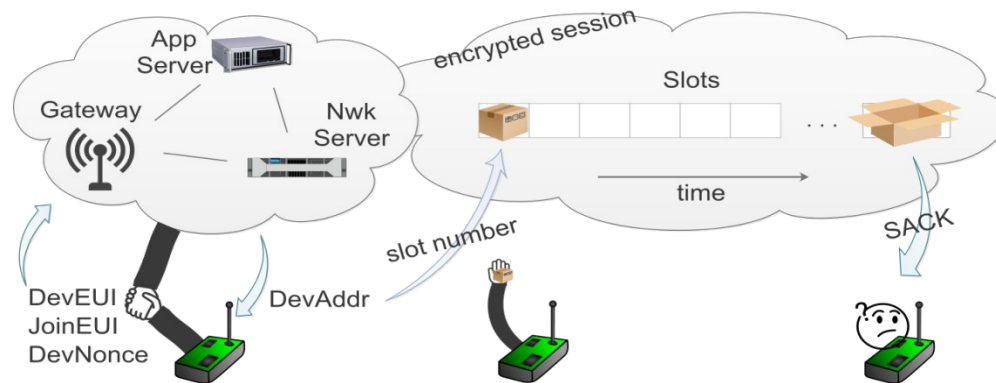
# Design Considerations

- **Radio duty cycle**

- **Uneven slot length**

- Delay / Application duty cycle

- Acknowledgements

- Scheduling

- Synchronisation

- Battery lifetime

- Propagation time

- Security

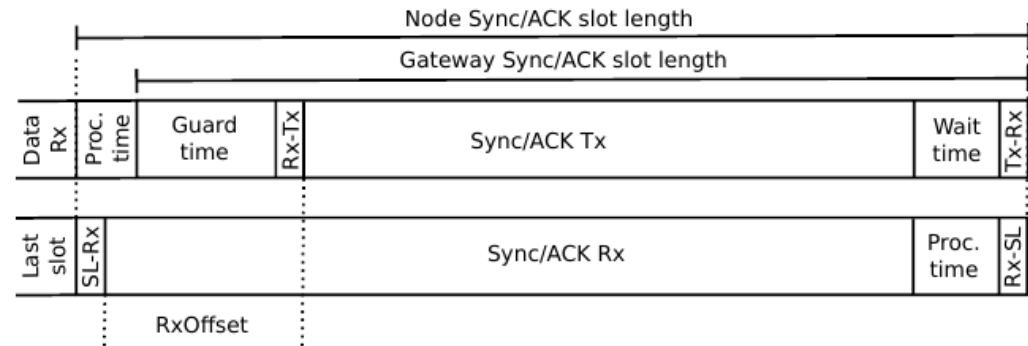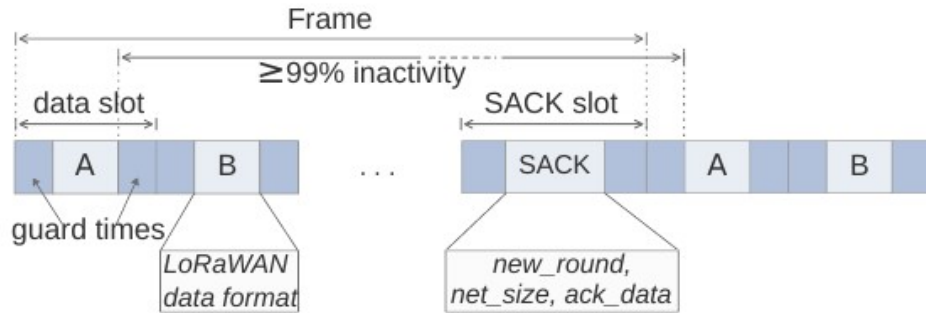| Frequency | | TP | Duty Cycle |
|---|---|---|---|
| K | 863 – 865 MHz | 25 mW ERP | $\leq 0.1\%$ or LBT |
| L | 865 – 868 MHz | 25 mW ERP | $\leq 1\%$ or LBT |
| M | 868 – 868.6 MHz | 25 mW ERP | $\leq 1\%$ or LBT |
| N | 868.7 – 869.2 MHz | 25 mW ERP | $\leq 0.1\%$ or LBT |
| O | 869.4 – 869.65 MHz | 500 mW ERP | $\leq 10\%$ or LBT |
| P | 869.7 – 870 MHz | 5 mW ERP | No requirement |
| Q | 869.7 – 870 MHz | 25 mW ERP | $\leq 1\%$ or LBT |
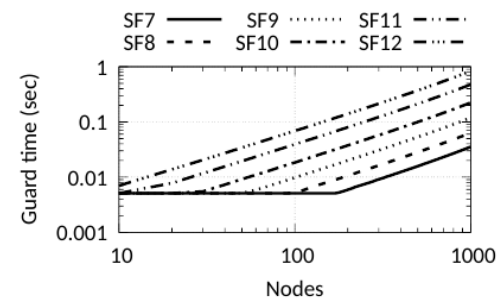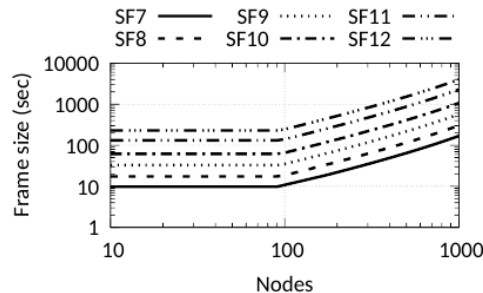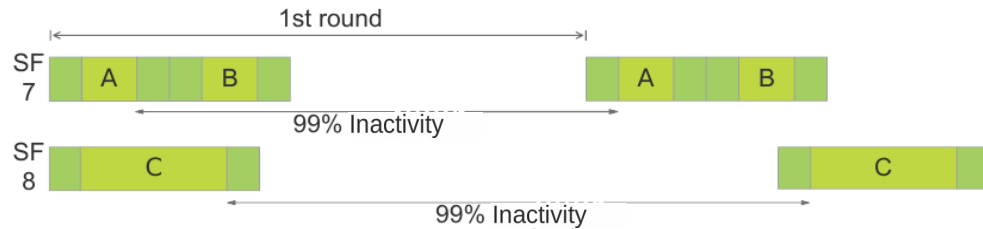
# TS-LoRa [1]

- Collision-free slot generation mechanism

- Autonomous slot assignment during the OTAA registration



[1] D. Zorbas, K. Abdelfadeel, P. Kotzanikolaou, D. Pesch, "TS-LoRa: Time-Slotted LoRa(WAN) for the Industrial Internet of Things", *Computer Communications*, Vol. 153, Mar. 2020, pp. 1-10
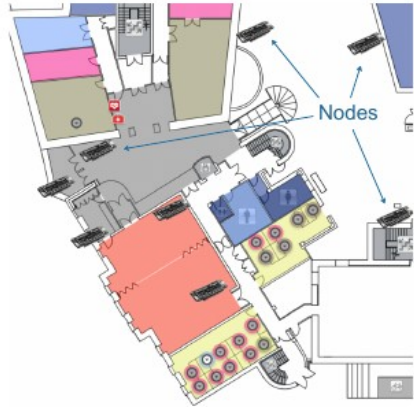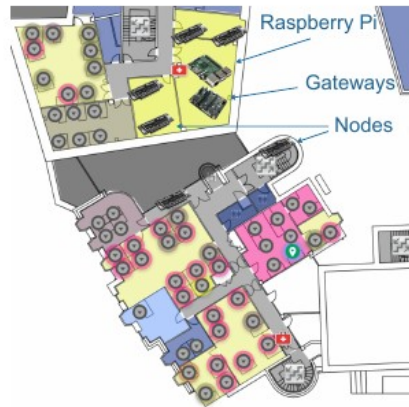
# TS-LoRa frame structure

- Multiple parallel frame structure + a SACK slot

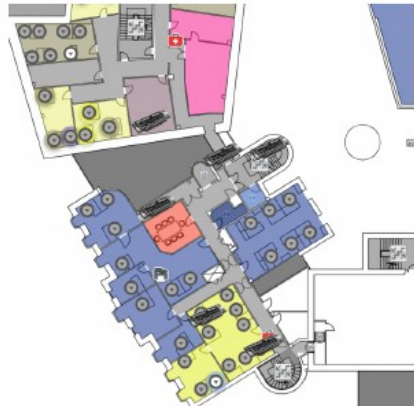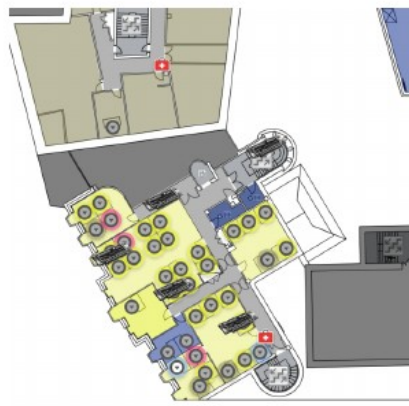  ○ SACK = Synchronisation and Acknowledgements

# Implementation [2]


(a) Ground floor


(b) 1st floor


(c) 2nd floor


(d) 3rd floor
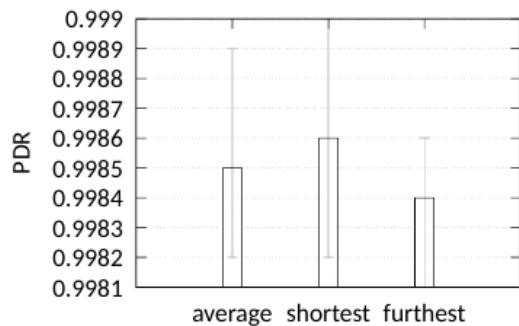
- 25 nodes
- SF7-9, 125kHz
- 100bytes packet size

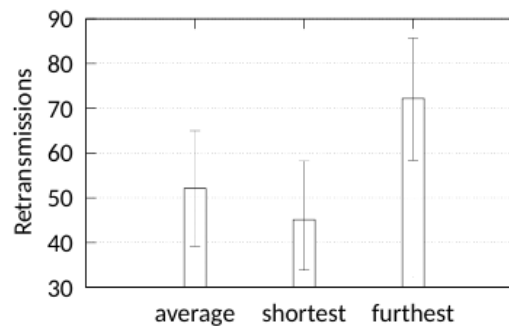| Frequency | SF | Duty Cycle |
|---|---|---|
| 865.0 − 865.5 MHz | 7 | ≤ 1% |
| 865.6 − 866.1 MHz | 8 | ≤ 1% |
| 866.2 − 866.7 MHz | 9 | ≤ 1% |
| 866.8 − 867.3 MHz | 10 | ≤ 1% |
| 867.4 − 867.9 MHz | 11 | ≤ 1% |
| 868.0 − 868.5 MHz | 12 | ≤ 1% |

[2] https://github.com/deltazita/ts-lora
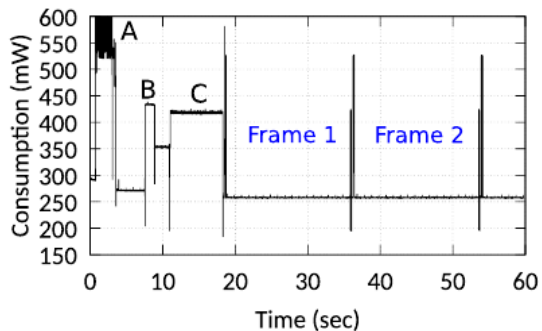
# Results [1]
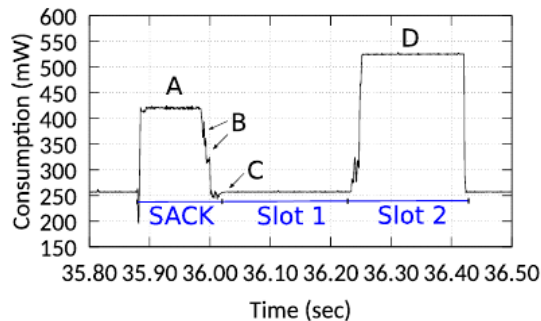
Experiments →
↓



(a) PDR



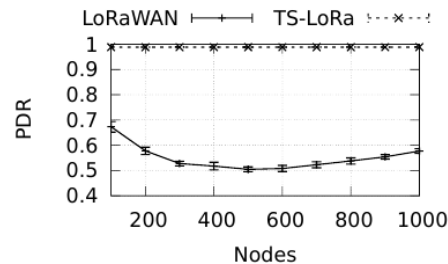(b) Number of retransmissions

Simulations ↓



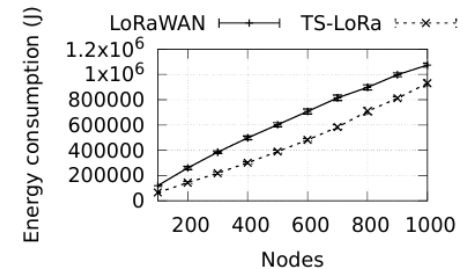(a) First minute: (A) node initialisation, (B) join request, (C) synchronisation waiting time



(b) SACK reception and data transmission: (A) SACK reception, (B) SACK processing, (C) end of 1st frame, (D) data transmission of 2nd frame



(a) Packet Delivery Ratio



(b) Total Energy Consumption

# Thank you for your attention!

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